

VXS Routing Study

Routing of high speed interconnects

update

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update

evaluation of three cases

- ◆ Fabric Slots both at one end
 - ◆ routing layers increased a lot (comp. to preferred solution)
 - ◆ high speed trace length of 450mm to 500mm (18" to 20")
 - ◆ no detailed analysis done

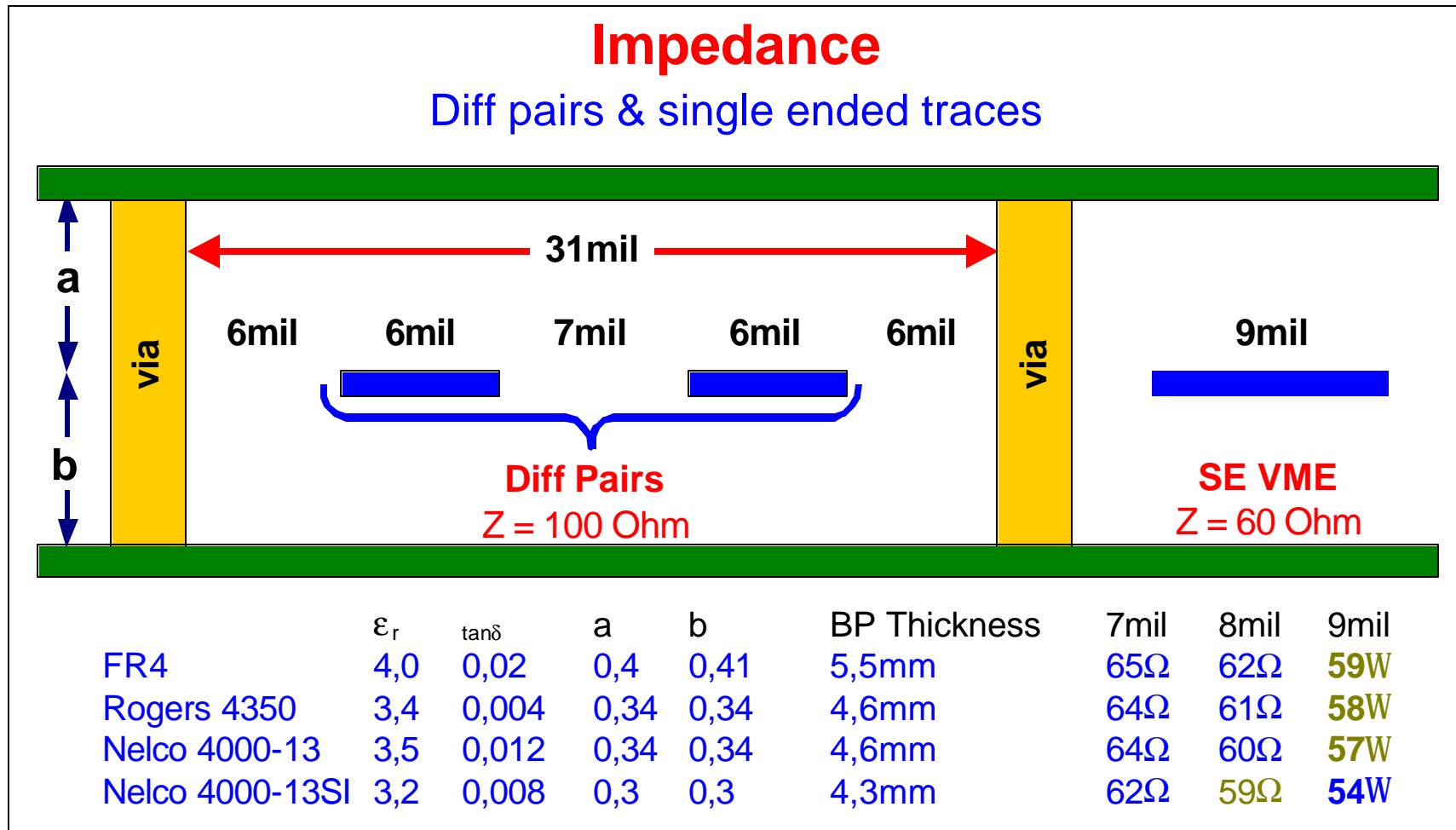
- ◆ Fabric Slots one left and one right
 - ◆ at least one routing layer more needed
 - ◆ high speed trace length of 450mm to 500mm (18" to 20")
 - ◆ no detailed analysis done

- ◆ Fabric Slots both in the middle
 - ◆ favored solution





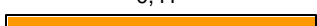

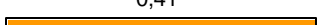

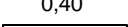
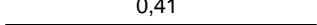
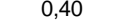

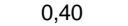
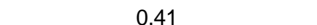
update

- ◆ 14 layers needed, 6 routing layers
- ◆ max high speed trace length 300mm (12")
- ◆ all nets routed: VXS (edge coupled diff. pairs) & VME)
- ◆ working now on fine tuning
 - ◆ **edge coupled lines**
 - ◆ **pro's:** only one layer per pair needed, better to integrate with traditional VME traces,
 - ◆ lower board thickness, less layers
 - ◆ **con's:** 6mil traces required (to pass MultiGig pins, pitch is 1,8mm)
 - ◆ **broadside coupled lines**
 - ◆ **pro's:** larger trace width possible (less skin losses)
 - ◆ **con's:** more layers needed, layer stack up doesn't harmonize with VME64x stack up
 - ◆ power distribution is poorer (patched power planes to keep layer numbers reasonable)

update



Layer stack up

VITA 41 Backplane Layer stack up			J1	J0	J2
Layer 1		Power			
Layer 2		Signal	VME	VXS	VME
Layer 3		Power			
Layer 4		Signal	VME	VXS	VXS
Layer 5		Power			
Layer 6		Signal	VME	VXS	VXS
Layer 7		Power			
Layer 8		Power			
Layer 9		Signal	VME	VXS	VXS
Layer 10		Power			
Layer 11		Signal	VXS	VXS	VXS
Layer 12		Power			
Layer 13		Signal	VXS	VXS	VXS
Layer 14		Power			

Overall Board Thickness: 5,5mm

- ◆ 2 VXS Layers
- ◆ 4 layers shared with VME on J1 / J2
 - ◆ VME J1 routed on 4 layers
 - ◆ VME J2 routed on 1 layers
- ◆ 6 Signal Layers total
- ◆ 8 power planes
- ◆ 5,5mm (216mil) board thickness
- ◆ Premises:
 - ◆ Signal Layers separated by Power Planes
 - ◆ Top & Bottom Layer should be no Signal Layers
 - ◆ symmetric stack up

Outlook

- ◆ all nets routed
- ◆ work on routing improvements (high speed traces)
- ◆ evaluations for higher speeds (VXS should run up to 10 Gbps!)
 - ◆ dielectric & skin losses
 - ◆ trace lengths
 - ◆ via-stubs ($\lambda/4$ filter, critical for > 5Gbps)
- ◆ target:
to know all issues effecting the backplane for up to 10 Gbps